ABSTRACT OF THE DISCLOSURE

A synchronous signal producing circuit includes an access inhibit region register for designating an access inhibit region for a processor in a shared memory, a comparing circuit for detecting the access by the processor to the access inhibit region designated in the access inhibit region register, and a logic circuit for issuing a P_DC signal setting the processor to a wait state based on a coprocessor instruction execution signal and a result of the comparison by the comparing circuit.